

1 CLAIMS:

2 1. A method of forming a conductive line comprising the
3 following steps:

4 forming a polysilicon layer;

5 forming a silicide layer against the polysilicon layer;

6 providing a conductivity-enhancing impurity within the silicide layer;

7 and

8 providing the polysilicon layer and the silicide layer into a
9 conductive line shape.

10
11 2. The method of claim 1 wherein the silicide comprises a
12 metal selected from the group consisting of tungsten, titanium,
13 molybdenum and cobalt.

14
15 3. The method of claim 1 wherein the steps of forming the
16 silicide layer and providing the conductivity-enhancing dopant therein
17 together comprise:

18 depositing a metal together with the conductivity-enhancing impurity
19 on the polysilicon layer; and

20 reacting the metal with the polysilicon to form the silicide layer
21 having the conductivity-enhancing impurity therein.
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1 4. The method of claim 1 wherein,
2 the step of forming the silicide layer comprises chemical vapor
3 depositing silicide on the polysilicon layer; and
4 the step of providing the conductivity enhancing impurity comprises
5 chemical vapor depositing the conductivity-enhancing impurity *in situ* with
6 the chemical vapor depositing of the silicide.

7
8 5. The method of claim 1 wherein,
9 the step of forming the silicide layer comprises chemical vapor
10 depositing a tungsten-comprising silicide on the polysilicon;
11 the step of providing the conductivity-enhancing impurity comprises
12 chemical vapor depositing the conductivity-enhancing impurity *in situ* with
13 the chemical vapor depositing of the tungsten-comprising silicide; and
14 the conductivity-enhancing impurity comprises a group III or a
15 group V element.

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17 6. The method of claim 5 wherein the step of chemical vapor
18 depositing the conductivity-enhancing impurity comprises utilizing a
19 precursor compound selected from the group consisting of PH_3 , AsH_3 ,
20 and diborane.

1 7. The method of claim 1 wherein the conductivity-enhancing
2 impurity is provided to a concentration of at least
3 about 1×10^{18} ions/cm³ within the silicide layer.
4

5 8. The method of claim 1 wherein the step of forming the
6 silicide layer and the step of doping the silicide layer together comprise:
7 providing a target comprising a metal, silicon and the conductivity-
8 enhancing impurity; and

9 sputtering of the target to form the silicide layer and the
10 conductivity-enhancing impurity within the silicide layer, the silicide layer
11 comprising the metal.
12

13 9. The method of claim 1 wherein the step of providing the
14 conductivity-enhancing impurity comprises:

15 ion implanting the conductivity-enhancing impurity into the silicide
16 layer after forming the silicide layer.
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18 10. The method of claim 1 wherein the polysilicon layer is doped
19 with the conductivity-enhancing impurity, and wherein the step of
20 providing the conductivity-enhancing impurity comprises:

21 out-diffusing the conductivity-enhancing impurity from the doped
22 polysilicon layer into the silicide layer.
23

1 11. The method of claim 1 wherein the step of providing the
2 conductivity-enhancing impurity comprises:

3 gas phase chemical doping of the silicide layer.
4

5 12. The method of claim 1 wherein the conductive line is a
6 wordline.
7

8 13. A method of lowering the resistivity of a metal-silicide layer
9 comprising doping the metal-silicide layer with a Group III dopant or a
10 Group V dopant.
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12 14. The method of claim 13 wherein the dopant is provided to
13 a concentration within the metal-silicide layer of at least
14 about 1×10^{18} ions/cm³.
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1 15. A method of forming a conductive line comprising the
2 following steps:

3 forming a polysilicon layer;

4 forming a silicide layer against the layer of polysilicon;

5 providing a conductivity-enhancing impurity within the silicide layer;

6 and

7 after providing the conductivity-enhancing impurity within the
8 silicide layer, subjecting the silicide layer to a processing step of over
9 850°C for at least 10 seconds.

10
11 16. The method of claim 15 wherein the forming the silicide
12 layer comprises depositing a metal layer over the polysilicon and reacting
13 the metal layer with the polysilicon, and wherein the conductivity-
14 enhancing impurity is provided within the metal layer prior to the
15 reacting the metal layer with the polysilicon.

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17 17. The method of claim 15 wherein the forming the silicide
18 layer comprises depositing a metal layer over the polysilicon and reacting
19 the metal layer with the polysilicon, and wherein the conductivity-
20 enhancing impurity is provided within the metal layer after the reacting
21 the metal layer with the polysilicon.
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1 18. The method of claim 15 wherein the conductivity-enhancing
2 impurity is implanted into the silicide layer.

3
4 19. The method of claim 15 wherein the conductivity-enhancing
5 impurity is provided to a concentration within the silicide layer of at
6 least about 1×10^{18} ions/cm³.

7
8 20. A method of forming a conductive line comprising the
9 following steps:

10 forming a polysilicon layer;

11 forming a silicide layer against the layer of polysilicon;

12 providing a conductivity-enhancing impurity within the silicide layer;

13 and

14 subjecting the silicide layer to a processing step of over 850°C for
15 at least 10 seconds while exposing the silicide layer to an oxygen-
16 comprising atmosphere.

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18 21. A conductive line comprising:

19 a polysilicon layer; and

20 a metal-silicide layer against the layer of polysilicon, the metal-
21 silicide layer comprising a Group III dopant or a Group V dopant.

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1 22. The conductive line of claim 21 wherein the metal-silicide
2 layer comprises a concentration of the dopant of at least
3 about 1×10^{18} ions/cm³.

4
5 23. A metal-silicide layer comprising a Group III dopant or a
6 Group V dopant.

7
8 24. The metal-silicide of claim 23 comprising a concentration of
9 the dopant of at least about 1×10^{18} ions/cm³.

10
11 25. A programmable-read-only-memory device comprising:
12 a first dielectric layer over a substrate;
13 a floating gate over the first dielectric layer;
14 a second dielectric layer over the floating gate;
15 a conductive line over the second dielectric layer; and
16 a metal-silicide layer over the conductive line, the metal-silicide
17 layer comprising a Group III dopant or a Group V dopant.

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19 26. The programmable-read-only-memory device of claim 25
20 wherein the device is an EPROM.
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1 27. The programmable-read-only-memory device of claim 25
2 wherein the device is an EEPROM.

3
4 28. The programmable-read-only-memory device of claim 25
5 wherein the metal-silicide layer comprises a concentration of the dopant
6 of at least about 1×10^{18} ions/cm³.

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8 add
9 B2